

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S68	5583	((438/202-208,234-239) or (257/E21.382-E21.385,E21.695-E21.696)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/19 10:04
S69	72	S68 and (poly near3 (silicon Si)) and ((mono single near3 (silicon Si) ) "a-Si") and bipolar	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/19 10:05
S70	18	("4808548"   "5017990"   "5106767"   "5107321"   "5144403"   "5439833"   "5580798"   "5599723"   "5607866"   "5661046"   "5940711"   "5953600"   "5986323"   "5986326"   "6028345"   "6316818"   "6465317"   "6492238").PN. OR ("6911681").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/04/19 10:27
S71	4666	pedestal with ("Si.O.sub.2" oxide silicon near3 (oxide ) insulat\$3 dielectric )	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/19 14:06
S72	62	S68 and S71	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/19 10:28
S74	345	S71 and bipolar	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/19 14:07
S75	24175	((257/552-562,E29.033) or (438/202-238,234-239,309-377) or (257/E27.015,E27.017,E27.03-E27.032,E27.109,E29.194-E29.225)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/24 13:42

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S76	927	S75 and (HBT hetero near3 bipolar)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/24 13:42
S77	42	S75 and (HBT hetero near3 bipolar) and ((single mono) near3 (crystal\$3 silicon)) and (poly near3 (crystal\$3 silicon))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/24 13:49
S79	1387	(438/309,312,315,316,317,338,342, 349).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/24 15:25
S80	179	S79 and (base emitter collect\$3) and (heterobipolar HBT hetero near3 bipolar) and ((mono single "a-") near3 (crystall\$3 silicon Si))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/24 15:44

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1670	((438/489) or (438/309,312,315,316, 317,318,319,338,342,349)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/26 18:18
L2	59	1 and (HBT heterobiopolar hetero near3 bipolar) and ((mono near3 (crystall\$3 Silicon Si) ) or (single near3 (crystall\$3 Silicon Si))) and (STI trench near3 isolat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 10:36
L3	231	(HBT heterobiopolar hetero near3 bipolar) and ((mono near3 (crystall\$3 Silicon Si) ) or (single near3 (crystall\$3 Silicon Si))) and (STI trench near3 isolat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 14:59
L4	172	3 not 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 13:44
L5	78	4 and (pedestal column)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 13:44
L7	418	(HBT heterobiopolar hetero near3 bipolar) and ((mono near3 (crystall\$3 Silicon Si SiGe (silicon near3 germanium)) ) or (single near3 (crystall\$3 Silicon Si) (silicon near3 germanium))) and (STI trench near3 isolat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 14:58
L8	246	7 not (4 or 5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 15:18

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L9	19	(hetero near3 bipolar heterobipolar HBT) and ((low near3 temperature) same (high near3 pressure) same oxidat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 15:20
L10	38	(hetero near3 bipolar heterobipolar HBT) and (((low near3 temperature) same (high near3 pressure) same oxidat\$3) or HIPOX)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/04/26 20:04
L12	1117	(257/552,554,557).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/26 18:19
L14	1410	(438/489,309,312,316,318,349).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/04/26 20:17
L15	0	((hetero near3 bipolar heterobipolar HBT) and ((single mono) near3 (Silicon Si (silicon near3 Germanium) SiGe crystall\$3)) and (poly near3 (Silicon (silicon near3 Germanium) SiGe crystall\$3)) and pedestal and base).clm.	US-PGPUB	OR	ON	2007/04/26 20:19
L16	0	((hetero near3 bipolar heterobipolar HBT) and ((single mono) near3 (Silicon Si (silicon near3 Germanium) SiGe crystall\$3)) and (poly near3 (Silicon (silicon near3 Germanium) SiGe crystall\$3)) and pedestal).clm.	US-PGPUB	OR	ON	2007/04/26 20:19
L17	6	((hetero near3 bipolar heterobipolar HBT) and pedestal).clm.	US-PGPUB	OR	ON	2007/04/26 20:20
L18	6	((hetero near3 bipolar heterobipolar HBT) and pedestal).clm.	US-PGPUB	OR	ON	2007/04/26 20:20

US-PAT-NO: 6888221

DOCUMENT-IDENTIFIER: US 6888221 B1

TITLE: BICMOS technology on SIMOX wafers

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Brief Summary Text - BSTX (6):

Other conventional HBT (heterojunction bipolar) devices utilize a LTE (low temperature epitaxy) SiGe (Silicon Germanium) base grown on silicon bounded by a STI (shallow trench isolation) region. Characteristics of these devices include a single-crystalline SiGe intrinsic base and a polycrystalline extrinsic base consisting of polysilicon over the STI region, which renders the resulting NPN (or PNP) geometry non-planar, and in fact quite bumpy. Also, there is a transitional faceted region disposed in between the intrinsic and extrinsic bases. However, this link region is highly resistive, which adversely impacts device performance. Moreover, for CMOS designers there remains a big challenge in optimizing the photolithography processes for these devices when the devices are scaled down.

Brief Summary Text - BSTX (8):

While, these devices were sufficient for the purposes they were designed, they do not provide optimum configurations for reducing the base resistance in the device. In addition, forming an isolation layer in Si substrates has been shown to be the most dominant approach in manufacturing due to the process simplicity. Therefore, due to the limitations of the conventional devices, there is a need for a practical and simple device and methodology that integrates SiGe HBTs with epitaxial extrinsic bases on SIMOX (separation by implanted oxygen) substrates and which overcomes the deficiencies of the conventional devices and methodologies.

Brief Summary Text - BSTX (14):

The invention relates to the state of the art CMOS technologies that are using SOI wafers. One main source of SOI wafers are from SIMOX. Building SiGe HBTs on SOI substrates takes advantage of the low power consumption of SOI technology and high current driverability of SiGe HBTs. The invention uses patterned SIMOX for BiCMOS isolation. This enables SiGe HBTs with planar structures. The invention achieves several advantages, such as a new and simple integration scheme that can be used for planar SiGe HBTs. Also, the invention achieves a much improved photolithography process on planar SiGe HBTs, especially as devices are scaled down. Moreover, the invention allows for reduced effect levels on planar SiGe HBTs and improves device yield. Moreover, according to the invention, CMOS are built at different regions on the same SIMOX wafers thereby providing a simple SiGe SOI technology.

Detailed Description Text - DETX (3):

As previously mentioned, there is a need for a practical and simple device and methodology that integrates SiGe **HBTs** on SIMOX substrates and which overcomes the deficiencies of the conventional devices and methodologies. Referring now to the drawings, and more particularly to FIGS. 1(a) through 5(d), there are shown preferred embodiments of the invention.

Detailed Description Text - DETX (8):

Next, in FIG. 1(k) **HIPOX** (High Pressure Oxidation) is performed whereby layer 32 is the silicon oxide layer that is converted from the polysilicon film 29 over the emitter. Here, thermal oxidation is carried out at the pressure of oxidizing ambient significantly higher than atmospheric pressure (e.g. 25 atm.), which allows fast growth of an oxide at reduced temperature. Then, the oxide layer 32 is removed as shown in FIG. 1(l). Next, FIG. 1(m) illustrates a second **HIPOX** layer 33 is converted from part of layer 30 outside the emitter pedestal region of emitter-base isolation. Thus, oxide 33 remains over the second monocrystalline layer 30.

Detailed Description Text - DETX (17):

The invention uses patterned SIMOX for BiCMOS isolation. This enables SiGe **HBTs** with planar structures. The invention achieves several advantages, such as a new and simple integration scheme that can be used for planar SiGe **HBTs**. Also, the invention achieves a much improved photolithography process on planar SiGe **HBTs**, especially as devices are scaled down. Moreover, the invention allows for reduced effect levels on planar SiGe **HBTs** and improves device yield. Moreover, according to the invention, CMOS are built at different regions on the same SIMOX wafers thereby providing a simple SiGe SOI technology.